What Is Claimed Is:

1. A semiconductor device having a non-volatile memory transistor, the semiconductor device comprising:

an interlayer dielectric layer provided on a semiconductor layer in which the non-volatile memory transistor is formed,

wherein the interlayer dielectric layer is an insulation layer for electrically isolating the non-volatile memory transistor from a conductive layer formed over the semiconductor layer, and the interlayer dielectric layer includes a layer containing nitride.

2. A semiconductor device according to claim 1, wherein the layer containing nitride is provided as a lowermost layer of the interlayer dielectric layer.

3. A semiconductor device according to claim 1, wherein the layer containing nitride is provided as an uppermost layer of the interlayer dielectric layer.

4. A semiconductor device according to claim 1, wherein the layer containing nitride is provided as an intermediate layer of the interlayer dielectric layer.

5. A semiconductor device according to claim 1, wherein the nitride is at least one of silicon nitride and silicon oxide nitride.

6. A semiconductor device according to claim 1, wherein the non-volatile memory transistor includes:

a floating gate disposed over the semiconductor layer through a gate dielectric layer;

a tunneling dielectric layer that contacts at least a part of the floating gate;

a control gate that is formed over the tunneling dielectric layer; and

source region and drain region formed in the semiconductor layer.

7. A semiconductor device according to claim 1, wherein the non-volatile memory transistor includes:

a floating gate disposed over the semiconductor layer through a gate dielectric layer;

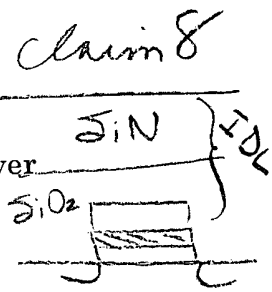
a control gate disposed over the floating gate through an intermediate dielectric layer; and

source region and drain region formed in the semiconductor layer.

8. A semiconductor device having a non-volatile memory transistor formed on a semiconductor layer, the semiconductor device comprising:

an interlayer dielectric layer provided over the semiconductor layer and the non-volatile memory transistor,

wherein the interlayer dielectric layer includes an oxide film provided as a lowermost layer of the interlayer dielectric layer and a layer containing nitride provided on the oxide film.



9. A semiconductor device according to claim 8, wherein the oxide film has a thickness of 10 – 80nm.

10. A semiconductor device according to claim 8, wherein the oxide film has a thickness of 30 – 70nm.

11. A semiconductor device according to claim 8, wherein the oxide film is an oxide film that is formed by a reduced pressure CVD method using TEOS.

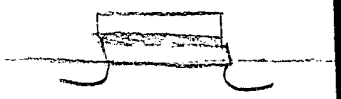
12. A method for manufacturing a semiconductor device, comprising the steps of:

(a) forming a non-volatile memory transistor in a semiconductor layer; and

(b) forming an interlayer dielectric layer over the semiconductor layer in which the non-volatile memory transistor,

wherein the interlayer dielectric layer is an insulation layer for electrically isolating a conductive layer formed over the semiconductor layer from the non-volatile memory transistor, and the interlayer dielectric layer includes a layer containing a nitride.

Claim 12
SiN IDL



13. A method for manufacturing a semiconductor device according to claim 12, wherein the layer containing nitride is provided as a lowermost layer of the interlayer dielectric layer.

14. A method for manufacturing a semiconductor device according to claim 12, wherein the layer containing nitride is provided as an uppermost layer of the interlayer dielectric layer.

15. A method for manufacturing a semiconductor device according to claim 12, wherein the layer containing nitride is provided as an intermediate layer of the interlayer dielectric layer.

16. A method for manufacturing a semiconductor device according to claim 12, wherein the nitride is at least one of silicon nitride and silicon oxide nitride.

17. A method for manufacturing a semiconductor device according to claim 12, wherein the non-volatile memory transistor includes:

a floating gate disposed over the semiconductor layer through a gate dielectric layer;

a tunneling dielectric layer that contacts at least a part of the floating gate;

a control gate that is formed over the tunneling dielectric layer; and

source region and drain region formed in the semiconductor layer.

18. A method for manufacturing a semiconductor device according to claim 12, wherein the non-volatile memory transistor includes:

a floating gate disposed over the semiconductor layer through a gate dielectric layer;

a control gate disposed over the floating gate through an intermediate dielectric layer; and

source region and drain region formed in the semiconductor layer.